The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a mask comprising a resist over the semiconductor to overlap with a portion of the semiconductor; and

adding an impurity element to the semiconductor in accordance with the mask by a doping method; and

wherein an area of the mask is at most 15% of an area of the substrate.

2. (Original) A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a mask comprising a resist over the semiconductor to overlap with a portion of the semiconductor; and

adding an impurity element to the semiconductor in accordance with the mask by a doping method with acceleration voltage of at least 80kV;

wherein an area of the mask is at most 15% of an area of the substrate.

3. (Currently Amended) A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer over a substrate;

forming a first mask comprising a resist over the second semiconductor ~~to overlap with a portion of the semiconductor; and~~ layer;

adding [[an]] a first impurity element having one conductivity to the first semiconductor layer in accordance with the first mask by a doping method;

removing the first mask;

forming a second mask comprising a resist over the first semiconductor layer; and

adding a second impurity element having a conductivity different from the one conductivity to the second semiconductor layer in accordance with the second mask,

wherein an area of at least one of the first mask and the second mask is at most 35% of an area of the substrate.

4. (Original) A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a mask comprising a resist over the semiconductor to overlap with a portion of the semiconductor and heating the resulted mask; and

adding an impurity element to the semiconductor in accordance with the mask by a doping method with acceleration voltage of at least 80kV;

wherein an area of the mask is at most 35% of an area of the substrate.

5. (Currently Amended) A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer over a substrate;

forming a first gate electrode over the first semiconductor ~~via an insulating film~~ layer with a first gate insulator therebetween;

forming a second gate electrode over the second semiconductor layer with a second gate insulator therebetween;

forming a first mask comprising a resist ~~in a position to overlap with a portion of the semiconductor~~ over the second semiconductor layer;

adding an n-type impurity element to the first semiconductor layer in accordance with the first mask and the first gate electrode by a doping method with acceleration voltage of at least 60kV;

removing the first mask;

forming a second mask comprising a resist ~~in a position to overlap with a portion of the semiconductor~~ over the first semiconductor layer; and

adding a p-type impurity element to the second semiconductor layer in accordance with the second mask and the second gate electrode by a doping method with acceleration voltage of at least 80kV;

wherein an area of the first mask is at most 20% of an area of the substrate, and an area of the second mask is at most 15% of an area of the substrate.

6. (Currently Amended) A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer over a substrate;

forming a first gate electrode over the first semiconductor ~~via an insulating film~~ layer with a first gate insulator therebetween;

forming a second gate electrode over the second semiconductor layer with a second gate insulator therebetween;

forming a first mask comprising a resist ~~in a position to overlap with a portion of the semiconductor~~ over the second semiconductor layer and heating the resulted first mask;

adding an n-type impurity element to the first semiconductor layer in accordance with the first mask and the first gate electrode by a doping method with acceleration voltage of at least 60kV;

removing the first mask;

forming a second mask comprising a resist ~~in a position to overlap with a portion of the semiconductor~~ over the first semiconductor layer and heating the resulted second mask; and

adding a p-type impurity element to the second semiconductor layer in accordance with the second mask and the second gate electrode by a doping method with acceleration voltage of at least 80kV;

wherein an area of the first mask is at most 40% of an area of the substrate, and an area of the second mask is at most 35% of an area of the substrate.

7. (Currently Amended) A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer over a substrate;

forming a first gate electrode over the first semiconductor ~~via an insulating film~~ layer with a first gate insulator therebetween;

forming a second gate electrode over the second semiconductor layer with a second gate insulator therebetween;

forming a first mask comprising a resist ~~in a position to overlap with a portion of the semiconductor~~ over the second semiconductor layer;

adding an n-type impurity element to the first semiconductor layer in accordance with the first mask and the first gate electrode by a doping method with current density of at least 15$\mu A/cm^2$ and with acceleration voltage of at least 60kV;

removing the first mask;

forming a second mask comprising a resist ~~in a position to overlap with a portion of the semiconductor~~ over the first semiconductor layer; and

adding a p-type impurity element to the second semiconductor layer in accordance with the second mask and the second gate electrode by a doping method with current density of at least 15μA/cm^2 and with acceleration voltage of at least 80kV;

wherein an area of the first mask is at most 20% of an area of the substrate, and an area of the second mask is at most 15% of an area of the substrate.

8. (Currently Amended) A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer over a substrate;

forming a first gate electrode over the first semiconductor ~~via an insulating film~~ layer with a first gate insulator therebetween;

forming a second gate electrode over the second semiconductor layer with a second gate insulator therebetween;

forming a first mask comprising a resist ~~in a position to overlap with a portion of the semiconductor~~ over the second semiconductor layer and heating the resulted first mask;

adding an n-type impurity element to the first semiconductor layer in accordance with the first mask and the first gate electrode by a doping method with current density of at least 15μA/cm^2 and with acceleration voltage of at least 60kV;

removing the first mask;

forming a second mask comprising a resist ~~in a position to overlap with a portion of the semiconductor~~ over the first semiconductor layer and heating the resulted second mask; and

adding a p-type impurity element to the second semiconductor layer in accordance with the second mask and the second gate electrode by a doping method with current density of at least 15μA/cm^2 and with acceleration voltage of at least 80kV;

wherein an area of the first mask is at most 40% of an area of the substrate, and an area of the second mask is at most 35% of an area of the substrate.

9.-11. (Canceled)

12. (Original) A method for manufacturing a semiconductor apparatus according to claim 1, wherein the semiconductor apparatus is a display device.

13. (Original) A method for manufacturing a semiconductor apparatus according to claim 2, wherein the semiconductor apparatus is a display device.

14. (Original) A method for manufacturing a semiconductor apparatus according to claim 3, wherein the semiconductor apparatus is a display device.

15. (Original) A method for manufacturing a semiconductor apparatus according to claim 4, wherein the semiconductor apparatus is a display device.

16. (Original) A method for manufacturing a semiconductor apparatus according to claim 5, wherein the semiconductor apparatus is a display device.

17. (Original) A method for manufacturing a semiconductor apparatus according to claim 6, wherein the semiconductor apparatus is a display device.

18. (Original) A method for manufacturing a semiconductor apparatus according to claim 7, wherein the semiconductor apparatus is a display device.

19. (Original) A method for manufacturing a semiconductor apparatus according to claim 8, wherein the semiconductor apparatus is a display device.

20. (Previously Presented) A method for manufacturing a semiconductor apparatus according to claim 12, wherein an area of the substrate is no less than 1 square meter.

21. (Previously Presented) A method for manufacturing a semiconductor apparatus according to claim 13, wherein an area of the substrate is no less than 1 square meter.

22. (Previously Presented) A method for manufacturing a semiconductor apparatus according to claim 14, wherein an area of the substrate is no less than 1 square meter.

23. (Previously Presented) A method for manufacturing a semiconductor apparatus according to claim 15, wherein an area of the substrate is no less than 1 square meter.

24. (Previously Presented) A method for manufacturing a semiconductor apparatus according to claim 16, wherein an area of the substrate is no less than 1 square meter.

25. (Previously Presented) A method for manufacturing a semiconductor apparatus according to claim 17, wherein an area of the substrate is no less than 1 square meter.

26. (Previously Presented) A method for manufacturing a semiconductor apparatus according to claim 18, wherein an area of the substrate is no less than 1 square meter.

27. (Previously Presented) A method for manufacturing a semiconductor apparatus according to claim 19, wherein an area of the substrate is no less than 1 square meter.